

**In the Specification:**

Please amend Paragraphs 0029, 0037 and 0045 as indicated below.

[0029] The second secondary winding  $L_{sec2}$  is coupled via a rectifier diode  $D_1$  to a capacitor  $C_2$  across which, in operation, a voltage difference  $V_{out2}$  is generated. Similarly, the first secondary winding  $L_{sec1}$  is connected in series with a capacitor  $C_1$  ~~[[C<sub>2</sub>]]~~ and a secondary field effect transistor switch FET SW2 as shown; in operation, a voltage difference  $V_{out1}$  is developed across the capacitor  $C_1$ . An output junction whereat the primary winding  $L_{prim}$  is coupled to the primary switch FET SW1 defines a voltage difference  $V_{prim}$  as illustrated. Likewise, an output junction whereat the first secondary winding  $L_{sec1}$  is connected to the secondary switch FET SW2 defines an output voltage  $V_{sec}$  which is coupled to a hard switching amplitude detector (SW DET) 20; the switching detector 20 includes, amongst other components, a sample-and-hold circuit whose operation is susceptible to being precisely time gated. The secondary switch FET SW2 is driven from a Q output of a flip-flop 35 whose reset input R is coupled to a circuit (not shown) operable to switch the switch FET SW2 to a non-conducting off state when a magnetizing current  $I_{magn}$  is less than a reference current  $I_{ref}$ ; the current  $I_{magn}$  is defined later. Moreover, the flip-flop 35 includes a set input S coupled to a start secondary stroke (ST. SEC. STR.) line for causing the secondary switch FET SW2 to conduct in an on state when this line assumes a logic 1 state.

[0037] In a conventional bidifly-type converter, the inventor has appreciated that it is desirable to discriminate between ringing that occurs after switchon of the primary switch FET SW1 from a steep slope, for example as represented by 70 in FIG. 2, arising at an instance the primary switch FET SW1 is driven to its conducting state, for example as represented by 75 in FIG. 2. In order to provide such discrimination, it would be conventionally anticipated that precise timing signals would need to be provided within the supply 10. As timing signals associated with the primary switch FET SW1 are available in the supply 10, these signals are beneficially employed for measuring the hard switching amplitude and ~~has~~ have been previously investigated by the inventor in the context of televisions and related visual monitor units.

[0045] In order to further elucidate the invention, an embodiment thereof will now be described with reference to FIG. 5. In FIG. 5, there is shown the supply [[10]] including its transformer TR1 with its first secondary winding  $L_{sec1}$  together with the aforementioned capacitor  $C_1$ , its secondary switch FET SW2 coupled to its corresponding flip-flop 35. The supply [[10]] in FIG. 5 is also providing with a hard switching amplitude detector indicated generally by 300 and included within a dashed line 305. The detector 300 comprises an imperfect differentiator 310, a temporally-gate integrator 320 and a control unit 330 for providing temporal gating signals DISDIF, DISINT to the differentiator 310 and to the integrator 320 respectively. An output signal line  $V_{hard}$  from the integrator 320 is arranged to provide a measure of hard switching amplitude arising in the primary switch FET SW1 during operation. The signals DISDIF, DISINT are arranged to be capable of resetting the differentiator 310 and the integrator 320 respectively. Moreover, the control unit 330 is provided with an input signal line HSE for receiving a signal generally indicative of a time interval in which hard switch is expected but not temporally exact in contradistinction to the prior art.